**ECE324 Homework2: Dataflow model**

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| **Exercise** | **Course outcome** | | **Grade** |
| Homework2 | | 2.a, 7.b | /30 |

2.a. Define engineering problems from specified needs for digital systems including implementation on FPGAs using HDL programming.

7.b. Employ appropriate learning strategies such as communicating with an expert, using external resources, experimentation, simulation, etc.

**Introduction:**

This homework assignment was to make a variable shifter given a 3-bit input select to determine how many bits to shift. The shifter contains 8 bits of data and outputs the 8 bits shifted by 0-7 bits.

**Shifter Module:**

The module is really simple. Built into Vivado in SystemVerilog, there are logical shift operators. This operator does most of the heavy lifting and all that’s left to do is specify what needs to be shifted (data input) and by how much (shift input). This is assigned to the shout output with one line and is ready to go to the test bench.

**Results:**

While the results below (Figure 1) look messy, they are easy to follow when realizing the inputs alternate between two different data values (0b00001111 and 0b11001100). For each pair of inputs, the test bench increments the shift value by one to test all possible combinations of shift values and the output verifies for each input the output is shifted the corresponding amount. This verifies the module is working exactly as intended. Figure 1 is also included separately if it is not completely legible within this document.

![A close up of a computer

Description automatically generated]()

**Figure 1:** Test Bench Output; All Combinations of ‘shift’, Two Different ‘data’ Values

**Conclusion:**

This assignment was a great example of using operations like shift operations to manipulate bits. This can be applied to many other digital logic circuits including barrel shifters and will probably be very useful in future assignments.